IN THE CLAIMS

Please amend claims 9 and 13, and add new claims 22-48 as follows:

1. (Original) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a silicon controlled rectifier (SCR), for coupling between a supply line of the IC and ground;

a first trigger device for coupling from the supply line to a first gate of the SCR;

a first shunt resistor for coupling between the first gate and ground;

a first gate control circuit, for coupling between the supply line and ground, and for further coupling to the first gate of the SCR; and

a common control circuit, for coupling between the supply line and ground, and for further coupling to the first gate control circuit.

2. (Original) The ESD protection circuit of claim 1, wherein said first gate control circuit comprises:

a first NMOS transistor having the drain coupled to the first gate and the source coupled to ground; and

a first inverter having an input and an output, wherein the output of said inverter is coupled to the gate of the first NMOS transistor and the common control circuit; and

wherein the first NMOS transistor provides a variable shunt element for the first trigger gate of the SCR.

3. (Original) The ESD protection circuit of claim 2, wherein said first inverter comprises:

a first PMOS transistor and a second NMOS transistor, and said first PMOS transistor and second NMOS transistor are serially coupled between the supply line and ground; and

the drains of said NMOS and PMOS transistors form an output of the inverter, wherein the output is connected to the gate of said first NMOS transistor.

4. (Original) The ESD protection circuit of claim 3, wherein said common control circuit

comprises:

a third NMOS transistor having the drain for coupling to the supply line, and the source coupled to an input of the inverter circuit;

a first pull-down resistor for coupling between the input of the inverter circuit and ground;

a trigger element for coupling between the supply line and the gate of the third NMOS transistor; and

a second pull-down resistor, for coupling between the gate of the third NMOS transistor and ground.

5. (Original) The ESD protection circuit of claim 4, wherein said trigger element is a device selected from the group consisting of a capacitor, a Zener diode coupled in a reverse bias direction between the supply line and the gate of the third NMOS transistor, and a grounded-gate NMOS transistor.

6. (Original) The ESD protection circuit of claim 4, further comprising:

a second trigger device for coupling from a second gate of the SCR to ground; and

a second gate control circuit for coupling between said supply line and said second gate, and further coupled to said common control circuit.

7. (Original) The ESD protection circuit of claim 5, wherein said second gate control circuit comprises a PMOS transistor having the source for coupling to said supply line, the drain coupled to said second trigger gate of the SCR, and the gate of the PMOS transistor coupled to the common control circuit.

8. (Original) The ESD protection circuit of claim 3, wherein said common control circuit comprises:

a second inverter having a second PMOS transistor serially coupled to a third NMOS transistor, said second inverter for coupling between the supply line and ground, and said inverter having an input and an output;

a pull-up resistor coupled to the input of said second inverter and the supply line; and

a fourth pull-down NMOS transistor having the drain coupled to the input of said second inverter and the source to ground, said gate of said fourth pull-down NMOS transistor coupled to the first gate of said SCR.

9. (Currently Amended) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a silicon controlled rectifier (SCR), for coupling between a protected supply line of the IC and a ground;

a first trigger device, for coupling from the said protected supply line to a first gate of the SCR;

a first shunt resistor coupled between the first gate and ground; and

~~a~~ an NMOS transistor[[,]] having ~~the~~ a drain and a source respectively[[,]] coupled between the first gate and ground, ~~and the gate of~~ said NMOS transistor having a gate for coupling to a supply line of the IC having a potential different from the potential of the protected supply line of the IC.

10. (Original) The ESD protection circuit of claim 9, further comprising:

a second trigger device coupled from a second gate of the SCR to ground.

11. (Original) The ESD protection circuit of claim 9, further comprising:

a PMOS transistor, having the source for coupling a supply line having a potential greater than the protected supply line, and the drain coupled to the second gate; and

the gate of said PMOS transistor for coupling to a supply line having a potential less than the potential of the supply line connected to the source of said PMOS.

12. (Original) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR, having a respective GGNMOS transistor coupled to a first gate of said

SCR, and a SGPMOS transistor coupled to a second gate of said SCR, said SCR, GGNMOS and SGPMOS transistors arranged in slices, further comprising:

an N-well;

a P-well positioned adjacent to said N-well and forming a junction therebetween;

a first plurality of P+ regions interspersed in said N-well forming an anode of said SCR, for coupling to a protected supply line, and a source of said SGPMOS transistor;

a first plurality of N+ regions interspersed in said P-well forming a cathode of said SCR, said first plurality of N+ regions for coupling to ground, and a source of said GGNMOS transistor, said first plurality of P+ and N+ regions being aligned and forming SCR and MOS transistor slices;

a second plurality of N+ regions interspersed in said N-well between said first plurality of P+ regions and forming a plurality of second gates and coupled to said anode;

a second plurality of P+ regions interspersed in said P-well between said first plurality of N+ regions and forming a plurality of first gates and coupled to said cathode; and

a third plurality of P+ regions interspersed in said N-well and separated from said first plurality of P+ regions by a respective first plurality of perpendicular gate regions, said third plurality of P+ regions forming a drain of said SGPMOS transistor; said first plurality of perpendicular gates coupled to said anode, said third plurality of P+ regions coupled to said cathode; and

a third plurality of N+ regions interspersed in said P-well and separated from said second plurality of N+ regions by a respective second plurality of perpendicular gate regions, said third plurality of N+ regions forming a drain of said GGNMOS transistor; said second plurality of perpendicular gates coupled to said cathode, said third plurality of N+ regions coupled to said anode.

13. (Currently Amended) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an N-well;

a P-well positioned adjacent to said N-well and forming a junction therebetween;

a first P+ region, forming a drain of a SGPMOS transistor disposed in said N-well, said first P+ region for coupling to ground;

a second P+ region forming an emitter of a PNP transistor of an SCR and forming a source of SGPMOS disposed in said N-well and parallel to said first P+ region, said second P+ region for coupling to a supply line of the IC;

a first gate region of said SGPMOS disposed parallel and between said first and second P+ regions, and over said N-well, said first gate region for coupling to the supply line of the IC;

a first N+ region, forming the second gate of an SCR disposed in said [[n-well]] N-well and parallel to said first and second P+ regions, said first N+ region for coupling to the supply line of the IC;

a second N+ region forming an emitter of an NPN transistor of said SCR and forming a source of a GGNMOS disposed in said P-well, ~~Said~~ said second N+ region for coupling to ground;

a third N+ region, forming a drain of a GGNMOS transistor disposed in said P-well parallel to said second N+ region, said third N+ region for coupling to the supply line of the IC;

a second gate region disposed in parallel and between said second and third N+ regions, over said P-well, said gate region for coupling to ground; and

a third P+ region, forming a second gate of the SCR disposed in said P-well and parallel to said second and third N+ regions, said third P+ region for coupling to ground.

14. (Original) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR, having a respective GGNMOS transistor having a parasitic NPN transistor having a the base coupled to a first gate of said SCR, said SCR and GGNMOS transistor arranged in slices, further comprising:

an N-well ;

a P-well, positioned adjacent to said N-well and forming a junction therebetween;

a first plurality of P+ regions interspersed in said N-well, and forming an emitter of a PNP transistor of said SCR and adapted for coupling to a supply line of the IC;

a first plurality of N+ regions interspersed in said N-well, and forming a drain contact region of said GGNMOS transistor, said first plurality of N+ regions for coupling to the supply line of the IC,

a second N+ region, disposed over said junction of said N-well and P-well, and coupling to said first plurality of N+ regions and forming drain of said GGNMOS transistor;

a third N+ region, forming an emitter of the NPN transistor and the source of said GGNMOS transistor, disposed in said P-well and parallel to said second N+ region, said third N+ region for coupling to ground;

a gate region, disposed in parallel and between said second and third N+ regions, over said P-well, and for coupling to ground;

a second P+ region, forming said first gate of said SCR, disposed in said P-well and parallel with said second and third N+ regions, said second P+ region for coupling to ground.

15. (Original) The ESD protection circuit of claim 14, further comprising:

a polysilicon layer disposed over said N-well and between the first P+ regions and the first interspersed N+ regions.

16. (Original) The ESD protection circuit of claim 14, wherein portions of the second and third N+ regions facing the gate region, and the gate region are silicide blocked.

17. (Original) The ESD protection circuit of claim 14, wherein said first interspersed N+ regions and third N+ region are segmented and resistor-ballasted, and said first and second P+ regions, said first, second, and third N+ regions, and said gate region are

fully silicided.

18. (Original) The ESD protection circuit of claim 14, further comprising a second N-well disposed below a portion of said third N+ region facing the second P+ region

19. (Original) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR having a respective GGNMOS transistor coupled to a first gate of said SCR, said SCR and GGNMOS transistor arranged in slices, further comprising:

an N-well having interdigited fingers;

a P-well having interdigited fingers, interlocking with said N-well fingers and forming a junction therebetween;

a first plurality of P+ regions disposed in each of the interdigitated fingers of said N-well, and forming an emitter of a PNP transistor of said SCR, and adapted for coupling to a supply line of the IC, said ;

a first plurality of N+ regions disposed in each of the interdigitated fingers of said P-well and forming a drain of said GGNMOS transistor, said first plurality of N+ regions coupled to the supply line,

a second N+ region disposed in said P-well and forming an emitter of the NPN transistor and the source of said GGNMOS transistor, said second N+ regions for coupling to ground;

a gate region, disposed in parallel and between said first plurality of interspersed N+ regions and the second N+ region, over said P-well, and adapted for coupling to ground;

a second P+ region, forming said first gate, disposed in said P-well and parallel with said second N+ region, and adapted for coupling to ground; and

a plurality of third P+ regions disposed in each of the interdigitated fingers of said P-well and between said first plurality of P+ regions and said first plurality of N+ regions, each third P+ region coupled to the gate region forming a local substrate pick-up.

20. (Original) The ESD protection circuit of claim 19, wherein a portion of the second and third N+ regions facing the gate region, and the gate region are silicide blocked.

21. (Original) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR comprising

a N-well;

a P-well positioned adjacent to said N-well and forming a junction therebetween;

a first plurality of P+ regions interspersed in said N-well forming an anode;

a first plurality of N+ regions interspersed in said P-well forming a cathode and aligned with said first plurality of P+ regions, each said first N+ region and first P+ region having a first length in a range from 0.16 to 10 micrometers;

a second plurality of P+ regions interspersed in said P-well between said first plurality of N+ regions and forming a plurality of first gates,

a second plurality of N+ regions interspersed in said N-well between said first plurality of P+ regions and forming a plurality of second gates; each said second N+ region and second P+ region having a second length in a range of 0.2 to 2 micrometers; and

wherein a distance between the first P+ region and the second N+ region are in a range from 0.12 to 1.2 micrometers, and a distance between the first N+ region and the second P+ regions are in a range from 0.12 to 1.2 micrometers.

22. (New) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a silicon controlled rectifier (SCR), for coupling between a first and a second supply line of the IC;

a trigger device for coupling a gate of the SCR to one of said first and second supply lines; and

a means for reducing an intrinsic resistance associated with said gate of the SCR.

23. (New) The ESD protection circuit of claim 22, wherein during powered-on operation of said IC, said means for reducing intrinsic resistance adapts a holding current to have a value greater than a current derived from a specified latch-up current for said IC.

24. (New) The ESD protection circuit of claim 23, wherein during powered-on operation of said IC, said means for reducing intrinsic resistance adapts a trigger current of said SCR to a value greater than a current derived from said specified latch-up current for said IC.

25. (New) The ESD protection circuit of claim 22, wherein during non-powered ESD operation of said IC, said means for reducing intrinsic resistance adapts a holding current of said SCR to a value less than a current derived from said specified latch-up current for said IC.

26. (New) The ESD protection circuit of claim 25, wherein during non-powered ESD operation of said IC, said means for reducing intrinsic resistance adapts a trigger current of said SCR to a value less than a current derived from said specified latch-up current for said IC.

27. (New) The ESD protection circuit of claim 22, wherein said means for reducing an intrinsic resistance comprises a resistive shunt formed in parallel to said intrinsic resistance.

28. (New) The ESD protection circuit of claim 22, wherein said means for reducing an intrinsic resistance comprises reducing a length of each of a plurality of first regions and a plurality of second regions respectively forming an anode and cathode of said SCR.

29. (New) The ESD protection circuit of claim 22, wherein said means for reducing an intrinsic resistance comprises reducing a length between of each of a plurality of regions forming trigger taps of said gate and at least one of an anode and cathode of

said SCR.

30. (New) The ESD protection circuit of claim 22, wherein said trigger device is coupled to a first gate of said SCR and said first supply line, said first supply line having a potential greater than said second supply line.

31. (New) The ESD protection circuit of claim 30, wherein said intrinsic resistance comprises a resistance of a substrate forming said first gate.

32. (New) The ESD protection circuit of claim 31, wherein said resistive shunt comprises a shunt resistor for coupling between the first gate and the second supply line.

33. (New) The ESD protection circuit of claim 30, wherein said first and second supply lines respectively comprise a positive voltage potential and ground.

34. (New) The ESD protection circuit of claim 22, wherein said trigger device is coupled to a second gate of said SCR and said second supply line, said first supply line having a potential greater than said second supply line.

35. (New) The ESD protection circuit of claim 34, wherein said intrinsic resistance comprises a resistance of an N-well forming said second gate.

36. (New) The ESD protection circuit of claim 35 wherein said resistive shunt comprises a shunt resistor for coupling between the second gate and the first supply line.

37. (New) The ESD protection circuit of claim 34 wherein said first and second supply lines respectively comprise a positive voltage supply and ground.

38. (New) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

a silicon controlled rectifier (SCR), for coupling between a supply line of the IC and a ground line;

a trigger device for coupling from the supply line to a second gate defined by an N-well of the SCR;

an N-well resistor for coupling between the second gate and the supply line; and

a shunt resistor for coupling between the second gate and the supply line, wherein said shunt resistor has a resistance value lower than the N-well resistor.

39. (New) The ESD protection circuit of claim 38, wherein the N-well resistor comprises an intrinsic resistance of the N-well of the protection circuit.

40. (New) The ESD protection circuit of claim 38, wherein the shunt resistor is selected from the group comprising a fixed resistor and a variable resistor.

41. (New) The ESD protection circuit of claim 38, wherein the trigger device comprises one of a grounded-gate NMOS device, a source-connected gate PMOS, a Zener diode in a reverse conduction direction, and a small diode chain in a forward conduction direction.

42. (New) The ESD protection circuit of claim 38, further comprising:

at least one diode, coupled in a forward conduction direction from a cathode of the SCR to ground.

43. (New) The ESD protection circuit of claim 38, further comprising:

a latch-up (LU) control circuit, for coupling between said supply line and ground, and further coupled to said second gate via said shunt resistor.

44. (New) The ESD protection circuit of claim 43, wherein the latch-up (LU) control circuit is further coupled to a reference supply line, which is coupled to ground via parasitic capacitance.

45. (New) The ESD protection circuit of claim 43, wherein said second gate comprises a plurality of second gates, said shunt resistor for coupling between said supply line and said plurality of second gates, and said second latch-up (LU) control circuit for further coupling to each second gate of each SCR finger via said shunt resistor.

46. (New) The ESD protection circuit of claim 38, wherein said shunt resistor adapts a holding current of said SCR to a value greater than a current derived from a specified latch-up current for said IC.

47. (New) The ESD protection circuit of claim 46, wherein said shunt resistor adapts a trigger current of said SCR to a value greater than a current derived from said specified latch-up current for said IC.

48. (New) An electrostatic discharge (ESD) protection circuit in a semiconductor integrated circuit (IC) having protected circuitry, comprising:

an SCR comprising

an N-well;

a P-well positioned adjacent to said N-well and forming a junction therebetween;

a first elongated P+ region disposed parallel to said junction in said N-well, said first elongated P+ region forming an anode of said SCR;

a first elongated N+ region disposed parallel to said junction and in said P-well, said first elongated N+ region forming a cathode of said SCR;

a second elongated P+ region disposed parallel to said first elongated P+ region in said P-well, said second elongated P+ region forming a first gate of said SCR;

a second elongated N+ region disposed parallel to said first elongated N+ region in said N-well, said second elongated N+ region forming a second gate of said SCR; and

wherein a distance between the first elongated P+ region and the second elongated N+ region is in a range from 0.12 to 1.2 micrometers, and a distance

between the first elongated N+ region and the second elongated P+ region is in a range from 0.12 to 1.2 micrometers.